

-SQA-SCOTTISH QUALIFICATIONS AUTHORITY

HIGHER NATIONAL UNIT SPECIFICATION

GENERAL INFORMATION

Unit Number	D3PK 04
Unit Title	COMBINATIONAL LOGIC AND CIRCUITS
Superclass Category	XL
Date of publication (month and year)	
Originating Centre for Unit	Cleveland Open Learning Unit

DESCRIPTION

On completion of this unit the candidate will be competent in designing, constructing and testing combinational logic circuits.

OUTCOMES:

1. interpret manufacture's data sheets for combinational logic devices;
2. design and test combinational logic circuits using discrete logic;
3. design and test combinational logic circuits using medium scale integration (m.s.i.) devices;
4. synthesize combinational logic using programmable devices.

CREDIT VALUE: 1 HN Credit

ACCESS STATEMENT:

Access to this unit is at the discretion of the centre. However, it would be beneficial if the student had competence in Boolean algebra and elementary logic. Evidence of this competence could be National Certificate Module 91061 Boolean Algebra or its equivalent.

Additional copies of this unit can be obtained from: The Administrative Services Unit, SQA, Hanover House, 24 Douglas Street, Glasgow G2 7NQ (Tel: 0141-242 2166).

At the time of publication, the cost is £2.50 (minimum order £5.00)

HIGHER NATIONAL UNIT SPECIFICATION**STATEMENT OF STANDARDS****Unit number:****Unit title:**

COMBINATIONAL LOGIC AND CIRCUITS

Acceptable performance in this Unit will be the satisfactory achievement of the standards set out in this part of the specification. All sections of the statement of the standards are mandatory and cannot be altered without reference to SQA.

OUTCOME**1. INTERPRET MANUFACTURER'S DATA SHEETS FOR COMBINATIONAL LOGIC DEVICES****PERFORMANCE CRITERIA**

- (a) Relating the performance of a logic device to its specification is correct in terms of the given parameters.
- (b) Comparisons of the performance of logic families are correct in terms of speed, power dissipation, cost and interface requirements.
- (c) Interpretation of the current National Standard for graphical symbols of binary logic elements is correct in terms of symbol outline, qualifying symbols and dependency notation.

RANGE STATEMENT

Performance:	fan-in; fan-out; noise margins; switching speed.
Parameters:	t_{PHL} ; t_{PLH} ; I_{IH} ; I_{IL} ; I_{OH} ; I_{OL} ; V_{IH} ; V_{IL} ; V_{OH} ; V_{OL} .
Symbol outline:	element outline; common control block; common output element.
General qualifying symbols:	AND; OR; XOR; code converter; multiplexer/demultiplexer; adder.
Input & output qualifying symbols:	negation; active-low input; active-low output; 3-state output; open-circuit output; enable input; bit-grouping.
Dependency notation:	EN; G; V.

EVIDENCE REQUIREMENTS

- PC (a) Written evidence that, given the appropriate parameters, the student can predict the given range of performance measurements for a particular device.
- PC (b) Written evidence to demonstrate the student's ability to interpret supplier's data so as to contrast the performance of different logic families and the problems associated in their interconnection.
- PC (c) Written and graphical evidence of the student's competence in the interpretation of the symbols as limited by the range statement.

OUTCOME

2. DESIGN AND TEST COMBINATIONAL LOGIC CIRCUITS USING DISCRETE LOGIC

PERFORMANCE CRITERIA

- (a) The laws and properties of Boolean algebra are applied correctly in the manipulation of expressions.
- (b) Methods used in the simplification of a Boolean function produce a minimal solution that meets the given specification.
- (c) The simplified Boolean function is represented correctly by a logic diagram implementing universal gates.
- (d) A circuit is designed and tested to meet a given specification.

RANGE STATEMENT

Laws: commutative; associative; distributive; duality; de Morgan.
Methods: algebraic; Karnaugh map.
Universal gates: NOR; NAND.

EVIDENCE REQUIREMENTS

Written evidence that the student can minimize a Boolean function involving up to and including four variables using appropriate algebraic and graphical techniques.

Performance evidence that the student can build the designed circuit using the prescribed type of universal gate (NAND or NOR) and demonstrate by truth table that its operation meets the given specification.

OUTCOME

3. DESIGN AND TEST COMBINATIONAL LOGIC CIRCUITS USING MEDIUM SCALE INTEGRATION (M.S.I.) DEVICES

PERFORMANCE CRITERIA

- (a) Graphical symbols for m.s.i. devices are correctly interpreted.
- (b) Combinational logic circuits are designed, built, tested and verified using the Boolean function generator properties of multiplexers and demultiplexers/decoders.

RANGE STATEMENT

m.s.i. devices: adder; multiplexer; demultiplexer/decoder; bcd-to-seven-segment decoder.

EVIDENCE REQUIREMENTS

- PC (a) Written evidence that the student can correctly interpret the symbol for each device in the range.
- PC (b) Two examples of performance evidence that the student can demonstrate the use of multiplexers and demultiplexers/decoders in the design, building and testing of m.s.i. solutions to combinational logic problems.

OUTCOME

4. SYNTHESIZE COMBINATIONAL LOGIC USING PROGRAMMABLE DEVICES

PERFORMANCE CRITERIA

- (a) The relative merits of using programmable logic devices as opposed to random logic are clearly identified.
- (b) The versatility of a programmable logic device is correctly related to its architecture.
- (c) Solutions presented to design problems involving programmable logic devices are correct in terms of pin allocations, input equations and fuse-map.

RANGE STATEMENT

Programmable logic device: PROM; PLA; PAL.

EVIDENCE REQUIREMENTS

- PC (a) Written evidence to demonstrate that the student appreciates the advantages of programmable devices.
- PC (b) Written evidence to show that the student knows of the relative complexities of the internal structures of the range of programmable devices and can associate this to their utility.
- PC (c) Written evidence to show that the student can produce design solutions to problems using at least two of the critical classes of the range. Performance evidence that the student can use a software package to generate a JEDEC file for a design solution involving a programmable logic device.

MERIT

To gain a pass in this unit, a candidate must meet the standards set out in the outcomes, performance criteria, range statements and evidence requirements.

To achieve a merit in this unit, a candidate must demonstrate a superior or more sophisticated level of performance. In this unit this might be shown in the following ways:

- (a) Demonstrating an ability to use a number of different performance criteria in an integrative way (e.g. to solve problems that are more complex than are necessary to demonstrate the achievement of the individual performance criteria).
- (b) Using the individual performance criteria in a creative way to solve unfamiliar problems, (i.e. is able to transfer a competence gained in one situation to be related but unfamiliar situation).
- (c) Demonstrating a critical awareness of the significance of the practical exercise to the theory and development of the subject.

ASSESSMENT

In order to achieve this unit, candidates are required to present sufficient evidence that they have met all the performance criteria for each outcome within the range specified. Details of these requirements are given for each outcome. The assessment instruments used should follow the general guidance offered by the SQA assessment model and an integrative approach to assessment is encouraged. (See references at the end of support notes.)

Accurate records should be made of the assessment instruments used showing how evidence is generated for each outcome and giving marking schemes and/or checklists, etc. Records of candidates' achievements should be kept. These records will be available for external verification.

SPECIAL NEEDS

Proposals to modify outcomes, range statements or agreed assessment arrangements should be discussed in the first place with the external verifier.

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SUPPORT NOTES

Unit Number

Unit Title

COMBINATIONAL LOGIC AND CIRCUITS

SUPPORT NOTES:

This part of the unit specification is offered as guidance. None of the sections of the support notes is mandatory.

NOTIONAL DESIGN LENGTH:

SQA allocates a notional design length to a unit on the basis of time estimated for achievement of the stated standards by a candidate whose starting point is as described in the access statement. The notional design length for this unit is 40 hours. The use of notional design length for programme design and timetabling is advisory only.

CONTENT/CONTEXT

The following information gives further clarification regarding the context in which the outcomes and performance criteria are to be achieved.

Corresponding to the outcomes:

1. BS3939 Part 12 (IEEE Standard 91-1984). An overview is intended, the more complicated symbols and dependencies being dealt with as they arise in subsequent outcomes.
2. Example of the use of a commercial software package as a design tool should, if possible, be given. Many manufacturers supply evaluation copies of software on CD-ROM or on the internet.
4. Evaluation copies of programming software are readily available from manufacturers over the internet.

REFERENCES

1. Guide to unit writing.
2. For a fuller discussion on assessment issues, please refer to SQA's Guide to Assessment.
3. Information for centres on SQA's operating procedures is contained in SQA's Guide to Procedures.
4. For details of other SQA publications, please consult SQA's publications list.

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