

-SQA-SCOTTISH QUALIFICATIONS AUTHORITY

HIGHER NATIONAL UNIT SPECIFICATION

GENERAL INFORMATION

Unit Number	D3PP 04
Unit Title	ELECTRONIC DEVICES
Superclass Category	XL
Date of publication (month and year)	
Originating Centre for Unit	Cleveland Open Learning Unit

DESCRIPTION

On completion of this unit the candidate will be competent in appraising the behaviour and application of a range of electronic devices.

OUTCOMES:

1. analyse the electrical behaviour of semiconductors;
2. apply semiconductor diode theory in practical applications;
3. apply bipolar transistor theory in practical applications;
4. apply field effect transistor theory in practical applications;
5. evaluate the properties and applications of optoelectronic devices.

CREDIT VALUE: 2 HN Credits

ACCESS STATEMENT:

Access to this unit is at the discretion of the Centre. However, it would be beneficial if the student has competence in mathematics, circuit theory and basic electronics. This may be evidenced by possession of National Certificate Module 'Analogue and Opto-Electronics' and HN Units 'Mathematics for Engineering' and 'Engineering Principles (Electrical)' or similar qualifications or experience.

Additional copies of this unit can be obtained from: The Administrative Services Unit, SQA, Hanover House, 24 Douglas Street, Glasgow G2 7NQ (Tel: 0141-242 2166).

At the time of publication, the cost is £2.50 (minimum order £5.00)

HIGHER NATIONAL UNIT SPECIFICATION
STATEMENT OF STANDARDS

Unit number:

Unit title: ELECTRONIC DEVICES

Acceptable performance in this Unit will be the satisfactory achievement of the standards set out in this part of the specification. All sections of the statement of the standards are mandatory and cannot be altered without reference to SQA.

OUTCOME

1. ANALYSE THE ELECTRICAL BEHAVIOUR OF SEMICONDUCTORS

PERFORMANCE CRITERIA

- (a) The classification of a material is determined from its variation of conductivity with temperature.
- (b) The law of mass action is correctly applied in relation to semiconductor carrier densities.
- (c) Analysis of the carrier mechanism in a semiconductor is valid in terms of the drift and diffusion equations, assuming linear density gradients and constant electric field.
- (d) The Fermi-Dirac energy distribution model is correctly applied to relate the effects of temperature and doping upon the shape of the probability distribution curve.
- (e) The variation of conductivity with temperature of both intrinsic and extrinsic semiconductor is correctly described within terms of the energy band model.

RANGE STATEMENT

Classification: conductor; insulator; semiconductor.

EVIDENCE REQUIREMENTS

Written evidence of the candidate's ability to describe, apply and analyse the effects and phenomena as detailed in PCs (a) to (e).

OUTCOME**2. APPLY SEMICONDUCTOR DIODE THEORY IN PRACTICAL APPLICATIONS****PERFORMANCE CRITERIA**

- (a) The properties and behaviour of semiconductor-semiconductor and semiconductor-metal junctions are correctly related to device structure and operating conditions by the appropriate models.
- (b) Comparison of the behaviour of an actual diode with that of a model diode is correct in terms of the diode equation.
- (c) Diode ratings and characteristics are correctly interpreted.
- (d) Diode performance is evaluated in rectifier and voltage reference applications.

RANGE STATEMENT

Diode:	rectifier; Schottky; Zener; avalanche.
Properties and behaviour:	ohmic; rectifying; depletion layer width; small signal (a.c.) resistance; large signal (d.c.) resistance; barrier potential; depletion layer junction capacitance; avalanche breakdown; Zener breakdown.
Device structure:	fabrication materials; geometry; doping.
Operating conditions:	applied voltage; temperature.
Models:	energy band diagram; parallel-plate capacitor; carrier density profile diagram (linear approximation); I/V characteristic.
Ratings and characteristics:	repetitive peak reverse voltage (V_{RRM}); working reverse voltage (V_{RW}); average forward current ($I_{F(AVE)}$); peak forward surge current (non repetitive) (I_{FSM}); reverse recovery time (t_r); thermal resistance ($R_{THj-case}$); maximum junction temperature (T_j); temperature coefficient (S_z).
Performance: Rectification:	forward volt drop; dynamic resistance; static resistance; simple thermal ($T = PR_{TH}$).
Voltage reference:	stabilization ratio; differential resistance.

EVIDENCE REQUIREMENTS

- PC (a) Written evidence of the candidate's ability to describe relationships between junction behaviour and structure/operating conditions by using the appropriate model.
- PC (b) Performance and written evidence of the candidate's ability to measure and compare with the ideal the characteristics of at least two types of diode.
- PC (c) Written or oral evidence of the candidate's ability to apply the range of data to problems and applications.
- PC (d) Performance evidence of the candidate's ability to measure the appropriate performance parameters of a rectifier diode and of a voltage reference diode.

OUTCOME**3. APPLY BIPOLAR TRANSISTOR THEORY IN PRACTICAL APPLICATIONS****PERFORMANCE CRITERIA**

- (a) The principles of operation of a bipolar transistor are correctly related to the given model.
- (b) The derivation and design application of the small signal parameters g_m and r_e are correct in relation to the exponential relationship between the base-emitter junction voltage and emitter current.
- (c) Transistor ratings and characteristics are correctly interpreted in relation to transistor circuit performance.
- (d) The principle features of an epitaxial planar transistor are correctly related to current manufacturing technology.
- (e) Measurements made to plot transistor output and transfer characteristics are accurate and the graphs are correct in terms of scale and annotation.
- (f) Predicted and measured performances of a single-stage common-emitter amplifier are compared.

RANGE STATEMENT

Model:	Ebers-Moll; energy-band diagram; h-parameter.
Ratings:	V_{CE0} ; I_C max; P_{tot} max.
Characteristics:	$V_{CE(SAT)}$; I_{CBO} ; f_T ; h_{fe} ; h_{FE} ; delay time; rise time; fall time; storage time.
Principal features:	junction isolation; oxide isolation; Schottky barrier diode; buried channel; ohmic junction.
Performance:	quiescent values; voltage gain; power gain; power conversion efficiency.

EVIDENCE REQUIREMENTS

- PC (a) One written example for each critical class of the candidate's ability to apply the model.
- PC (b) Written evidence that the candidate can derive the parameters and apply them correctly in a design example.
- PC (c) Written and or oral evidence that the candidate can interpret the range category of ratings and characteristics in relation to transistor circuit performance.
- PC (d) Written or oral evidence of the candidate's ability to relate the range of features to manufacturing technology.
- PC (e) Performance and graphical evidence of the candidate's ability to make the required measurements and correctly plot the characteristics.
- PC (f) Performance evidence of the candidate's ability to make the required measurements and, where appropriate, written evidence of comparison with calculated values.

OUTCOME**4. APPLY FIELD-EFFECT TRANSISTOR THEORY IN PRACTICAL APPLICATIONS****PERFORMANCE CRITERIA**

- (a) The principles of operation of a field-effect transistor are correctly related to the appropriate mathematical model.
- (b) Transistor ratings and characteristics are correctly interpreted.
- (c) Measurements made to plot transfer characteristics are accurate and the graph correct in terms of scale and annotation.
- (d) The switching properties of the MOSFET are demonstrated.
- (e) Measured performance of a single-stage FET amplifier is compared to that predicted from circuit and small-signal model analysis.

RANGE STATEMENT

Field effect transistors: JFET; MOSFET.

Mathematical Model: $I_{D(SAT)} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$ (JFET);

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2 \text{ (MOSFET)}$$

Ratings: P_{tot} ; V_{DS} ; V_{GS} ; I_G ; I_D .

Characteristics: V_{DS} ; V_T ; V_P ; $I_{D(SAT)}$; I_{DSS} ; y_{fs} ; g_{fs} ; source resistance r_s .

Performance: quiescent values; voltage gain.

EVIDENCE REQUIREMENTS

- PC (a) Written evidence of the candidate's understanding of the physical significance of the terms occurring in each model of the range.
- PC (b) Written and or oral evidence of the candidate's ability to interpret the range category of ratings and characteristics.
- PC (c) Performance evidence of the candidate's ability to measure and plot a transfer characteristic.
- PC (d) Performance evidence of the use of a MOSFET as a logic gate or other switching application.
- PC (e) Performance and written evidence of the candidate's ability to measure, calculate and compare the required values and parameters.

OUTCOME

5. EVALUATE THE PROPERTIES AND APPLICATIONS OF OPTOELECTRONIC DEVICES

PERFORMANCE CRITERIA

- (a) The solutions to problems relating the operation and performance of an optical fibre to its characteristics and light source are correct.
- (b) Analysis of the effects of light upon the conductivity of a doped semiconductor is correct in terms of the irradiance and wavelength of the light and the temperature and properties of the semiconductor.
- (c) The performance of an optoelectronic device is calculated given its physical properties and operating conditions.
- (d) The relative advantages of solid state displays are critically compared.
- (e) The advantages of using optical coupling are correctly stated.

RANGE STATEMENT

Optical fibre:	monomode; stepped index; graded index.
Fibre characteristics:	refractive index; modal dispersion; material dispersion; dispersion time; attenuation; numerical aperture; geometry; number of modes supported.
Light source:	spectral width; operating wavelength.
Semiconductor properties:	mobility; carrier density; quantum efficiency; carrier lifetime.
Optoelectronic device:	LED; phototransistor.
Performance:	optical power output (LED); collector current (phototransistor).
Physical properties:	energy gap; quantum efficiency; responsivity; spectral response.
Solid state displays:	LED; transmissive LCD; reflective LCD.

EVIDENCE REQUIREMENTS

- PC (a) Written evidence to the solution of problems to satisfy the performance criteria and range statements.
- PC (b) Written evidence that the candidate can explain and quantify the effects of light and thermal energy upon the conductivity a doped semiconductor.
- PC (c) Written evidence that the candidate can estimate the power output of an LED and the current in a phototransistor from given data.
- PC (d) & (e) Written or oral evidence to show the candidate is aware of the relative advantages.

MERIT

To gain a pass in this unit, a candidate must meet the standards set out in the outcomes, performance criteria, range statements and evidence requirements.

To achieve a merit in this unit, a candidate must demonstrate a superior or more sophisticated level of performance. In this unit this might be shown in the following ways:

- (a) Demonstrating an ability to use a number of different performance criteria in an integrative way (e.g. to solve problems that are more complex than are necessary to demonstrate the achievement of the individual performance criteria).
- (b) Using the individual performance criteria in a creative way to solve unfamiliar problems, (i.e. is able to transfer a competence gained in one situation to be related but unfamiliar situation).
- (c) Demonstrating a critical awareness of the significance of the practical exercise to the theory and development of the subject.

ASSESSMENT

In order to achieve this unit, candidates are required to present sufficient evidence that they have met all the performance criteria for each outcome within the range specified. Details of these requirements are given for each outcome. The assessment instruments used should follow the general guidance offered by the SQA assessment model and an integrative approach to assessment is encouraged. (See references at the end of support notes.)

Accurate records should be made of the assessment instruments used showing how evidence is generated for each outcome and giving marking schemes and/or checklists, etc. Records of candidates' achievements should be kept. These records will be available for external verification.

SPECIAL NEEDS

Proposals to modify outcomes, range statements or agreed assessment arrangements should be discussed in the first place with the external verifier.

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HIGHER NATIONAL UNIT SPECIFICATION**SUPPORT NOTES****Unit Number****Unit Title**

ELECTRONIC DEVICES

SUPPORT NOTES:

This part of the unit specification is offered as guidance. None of the sections of the support notes is mandatory.

NOTIONAL DESIGN LENGTH:

SQA allocates a notional design length to a unit on the basis of time estimated for achievement of the stated standards by a candidate whose starting point is as described in the access statement. The notional design length for this unit is 80 hours. The use of notional design length for programme design and timetabling is advisory only.

CONTENT/CONTEXT

The following information gives further clarification regarding the context in which the outcomes and performance criteria are to be achieved.

Corresponding to the outcomes:

1. (b) Law of mass action $np = n_i^2$

(c) $J = J_n + J_p$

where $J_n = en\mu_n E + eD_n \frac{dn}{dx}$

and $J_p = en\mu_p E - eD_p \frac{dp}{dx}$

and in the absence of diffusion

$$= e\mu_n E + e\mu_p E$$

- (d) A simple treatment of Fermi-Dirac distribution as derived from Boltzmann distribution is intended, culminating in an energy band diagram having a distribution curve symmetrical about the Fermi level. The effects of doping upon the position of the Fermi level should be included.

The probability equation should be given:

$$p(E) = \frac{1}{\exp \frac{E - E_F}{kT} + 1}$$

From which $p(E) \approx \exp \frac{-E_g}{2kT}$ for $E_g \gg kT$

- (e) Given that, for intrinsic semiconductors, charge carrier density is an exponential function of temperature ($n \approx \exp -\frac{E_g}{2kT}$) the variation of its conductivity with temperature can be determined. The variation of extrinsic material conductivity with temperature should be described qualitatively.
2. (a) The description of p-n junction operation should be given in terms of carrier diffusion and in terms of the energy band model.

Discussion of junction capacitance (transition region capacitance) under reverse bias, reverse breakdown and avalanche effect should be included.

For linear diffusion gradient model, the reverse current in a pn junction diode is related to the diffusion gradients and junction cross-sectional area by the equation:

$$I_R = eA \left(\frac{D_n n_p}{l_p} + \frac{D_p p_n}{l_n} \right)$$

For a Schottky diode (n-type semiconductor) the above equation becomes

$$I_R = eA \frac{D_n n_n}{l_n}$$

From these equations predictions of the effects of geometry, doping and temperature upon reverse current can be made.

The transition region width is related to the reverse bias by

$$w_t = \sqrt{V_R + V_D}$$

$$w_t = \sqrt{\frac{(V_R + V_D)}{e} \left(\frac{1}{N_a} + \frac{1}{N_d} \right)} \dots \dots \dots$$

Where V_D is the diffusion potential.

By the parallel-plate capacitor analogy, the transition region capacitance of a junction is given by:

$$C_t = \frac{A}{w_t}$$

Thus

$$C_t = \frac{1}{\sqrt{V_R + V_D}}$$

Junction breakdown voltage is proportional to the width of the transition region (the wider the region the lower the electric field). But equation (1) shows that higher levels of doping reduce the width of the transition region.

$$(b) \quad I_D = I_S \exp \frac{eV_D}{kt} - 1 \quad \text{from which} \quad r = \frac{25}{I}$$

The effect of temperature upon I_S should be stressed.

3. (a) The importance of base dimensions and doping levels for efficient operation should be identified.

$$(b) \quad I_C = I_E = I_{EBO} \exp \frac{eV_{BE}}{kT} \quad \text{for a forward biased EB junction}$$

from which the mutual conductance $g_m = \frac{dI_C}{dV_{BE}}$

is derived, i.e. $g_m = \frac{eI_C}{kT} = 40 I_C \text{ mS} (I_C \text{ in mA}),$

$$r_e = \frac{25}{I_E} \quad (I_E \text{ in mA}).$$

4. (a) Application should include the FET as a switch and its role in VLSI.

The four possible MOSFET configurations (n/p-channel, enhancement/depletion) to be included. Transfer and output characteristics for one type of device only. Ohmic and saturation regions. Pinch-off.

5. (a) Total internal reflection and critical angle are included.

- (b) The conductivity of a thin wafer of doped semiconductor which is exposed to a light of irradiance E , is given by:

$$= e (\mu_n n + \mu_p p) + \frac{qE}{hc} (\mu_n + \mu_p)$$

- (c) $= \frac{hc}{W_g}$ where W_g is the cut-off wavelength.

Unit No.

Continuation

The terms quantum efficiency and responsivity should be defined.

REFERENCES

1. Guide to unit writing.
2. For a fuller discussion on assessment issues, please refer to SQA's Guide to Assessment.
3. Information for centres on SQA's operating procedures is contained in SQA's Guide to Procedures.
4. For details of other SQA publications, please consult SQA's publications list.

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