

-SQA- SCOTTISH QUALIFICATIONS AUTHORITY

HIGHER NATIONAL UNIT SPECIFICATION

GENERAL INFORMATION

Unit Number	D3RC 04
Unit Title	SEQUENTIAL LOGIC AND CIRCUITS
Superclass Category	XL
Date of Publication (month and year)	
Originating Centre for Unit	Cleveland Open Learning Unit

DESCRIPTION

GENERAL COMPETENCE FOR UNIT:

Applying formal methods in the design of sequential logic systems.

OUTCOMES:

1. specify the properties of sequential logic circuits;
2. apply formal design techniques to synchronous sequential logic circuits;
3. implement sequential logic design projects using integrated circuit devices.

CREDIT VALUE: 1 HN Credit

ACCESS STATEMENT:

Access to this unit is at the discretion of the centre. It would be, however, beneficial if the student had competence in combinational logic design. Evidence of this competence could be the possession of the Higher National unit 'Combinational Logic and Circuits' or its equivalent.

Additional copies of this unit can be obtained from: The Administrative Services Unit, SQA, Hanover House, 24 Douglas Street, Glasgow G2 7NQ (Tel: 0141-242 2166).

At the time of publication, the cost is £2.50 (minimum order £5.00)

HIGHER NATIONAL UNIT SPECIFICATION**STATEMENT OF STANDARDS****Unit Number****Unit Title****SEQUENTIAL LOGIC AND CIRCUITS**

Acceptable performance in this Unit will be the satisfactory achievement of the standards set out in this part of the specification. All sections of the statement of the standards are mandatory and cannot be altered without reference to SQA.

OUTCOME**1. SPECIFY THE PROPERTIES OF SEQUENTIAL LOGIC CIRCUITS****PERFORMANCE CRITERIA**

- (a) Classification of sequential logic is correct in terms of synchronous and asynchronous working.
- (b) Interpretation of the current National Standard for graphical symbols of binary logic elements is correct.
- (c) The behaviour of a bistable element is correctly described using appropriate representation.
- (d) Integrated circuit packages are used to demonstrate the operation of J-K and type-D bistables.

RANGE STATEMENT

Symbol outline:	element outline; common control block; common output element
General qualifying symbols:	AND; OR; XOR; counter; shift register; retriggerable monostable ;
Input & output qualifying symbols:	negation; active-low input; active-low output; R; S; D; J; K; T; CT; shift; counting; bit-grouping (m1 - - - mk); enable input; dynamic inputs; postponed output
Dependency notation:	EN; G; V; N; S; R; M; C
Bistable element:	S-R flip-flop; type-D Flip-flop; type-T Flip-flop J-K flip-flop; master-slave J-K flip-flop.
Appropriate representation:	truth table; steering table; Karnaugh map; timing diagram.

EVIDENCE REQUIREMENTS

- PC (a) Written and or oral evidence to demonstrate that the student understands the meaning of and can differentiate between the two types of working .
- PC (b) Written and graphical evidence of competence in the interpretation of the symbols.
- PC (c) Written and graphical evidence to show that the student can illustrate the operation of the range of bistable elements by using one of the range of appropriate representations. An example of the use of each type of representation must given.
- PC (d) Performance evidence that the student can demonstrate the operation of each type of bistable by verifying its steering table.

OUTCOME**2. APPLY FORMAL DESIGN TECHNIQUES TO SYNCHRONOUS SEQUENTIAL LOGIC CIRCUITS**

PERFORMANCE CRITERIA

- (a) Sequential behaviour of a specification is verified by a state diagram from a given starting state and a sequence of input values.
- (b) A state-transition table is correctly constructed from a specification's state diagram.
- (c) The minimum number of binary elements is determined exactly from the number of internal system states.
- (d) Next-state and output functions are derived and minimized.
- (e) Logic diagrams are drawn correctly in terms of function and drawing convention.

RANGE STATEMENT

Logic circuits: four-stage synchronous counter; sequence detector; 4-bit shift register.
State diagram: Mealy model; Moore model.

EVIDENCE REQUIREMENTS

PC (a) Graphical evidence of a diagram of at least four nodes for each model.
PC (b) to (e) Three examples of written, tabular and graphical evidence to show that the student can apply the formal design techniques successfully in the production of logic diagrams for the range of circuits.

OUTCOME

3. IMPLEMENT SEQUENTIAL LOGIC DESIGN PROJECTS USING INTEGRATED CIRCUIT DEVICES

PERFORMANCE CRITERIA

- (a) Manufacturers' data for selected integrated circuit devices are correctly interpreted.
- (b) Block diagrams drawn for the proposed system accurately represent the required specification.
- (c) Supporting and driving logic requirements are derived from design equations.
- (d) The realised design is built, tested and verified as functioning according to specification.

RANGE STATEMENT

Integrated circuit devices: gates; flip-flops; m.s.i devices.

EVIDENCE REQUIREMENTS

Two different examples are required; at least one of which should incorporate the use of a m.s.i device. Oral, written and graphical evidence to show that the student can apply design rules and produce supporting documentation in the realization of a sequential logic system, as detailed by Performance Criteria (a), (b) and (c). PC (d) Performance evidence that the student can build, test and demonstrate the correct functioning of the system.

MERIT

To gain a pass in this unit, a candidate must meet the standards set out in the outcomes, performance criteria, range statements and evidence requirements.

To achieve a merit in this unit, a candidate must demonstrate a superior or more sophisticated level of performance. In this unit this might be shown in the following ways:

Unit No.

Continuation

- (a) using the individual performance criteria in a creative way to solve unfamiliar problems by the transfer a competence gained in one situation to be related but unfamiliar situation;
- (b) demonstrating a critical awareness of the relation of theory to the practical development of the subject when, for example implementing a sequential design;
- (c) research outwith the normal course content.

ASSESSMENT

In order to achieve this unit, candidates are required to present sufficient evidence that they have met all the performance criteria for each outcome within the range specified. Details of these requirements are given for each outcome. The assessment instruments used should follow the general guidance offered by the SQA assessment model and an integrative approach to assessment is encouraged. (See references at the end of support notes.)

Accurate records should be made of the assessment instruments used showing how evidence is generated for each outcome and giving marking schemes and/or checklists, etc. Records of candidates' achievements should be kept. These records will be available for external verification.

SPECIAL NEEDS

Proposals to modify outcomes, range statements or agreed assessment arrangements should be discussed in the first place with the external verifier.

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HIGHER NATIONAL UNIT SPECIFICATION

SUPPORT NOTES

Unit Number

Unit Title

SEQUENTIAL LOGIC AND CIRCUITS

SUPPORT NOTES:

This part of the unit specification is offered as guidance. None of the sections of the support notes is mandatory.

NOTIONAL DESIGN LENGTH:

SQA allocates a notional design length to a unit on the basis of time estimated for achievement of the stated standards by a candidate whose starting point is as described in the access statement. The notional design length for this unit is 40 hours. The use of notional design length for programme design and timetabling is advisory only.

CONTENT/CONTEXT

The following information gives further clarification regarding the context in which the outcomes and performance criteria are to be achieved.

Corresponding to the Outcome:

1. Timing hazards of asynchronous circuits should be identified.

BS 3939 Part 12 describes and defines binary logic elements. A good description is also given in the Texas Instruments TTL Data Book.
2. The relative merits of the Mealy and Moore models should be explained. The use of a software emulation package is greatly encouraged as a design aid. Demonstration versions of such software are available from manufacturer's on CD-Rom or via their web sites.
3. The two 'design and build' projects may be given or the students can suggest their own. It is intended that the student should apply design rules to build reasonably complex systems that incorporate several integrated circuits. At least one of the designs should include a m.s.i device such as a shift register, counter, error detection circuit, arithmetic circuit, multivibrator, etc. The finished product can be built on either a 'breadboard' or a p.c.b. Again, the use of a software emulation package will much enhance the design and testing cycle.

APPROACHES TO GENERATING EVIDENCE

A student-centred learning approach is recommended in which students have an early opportunity to reinforce theory by practice exercises. The more advanced symbols should be introduced and explained as they arise within the unit.

Where a candidate is unsuccessful in achieving an outcome, provision should be made for remedial work followed by reassessment.

ASSESSMENT PROCEDURES

Centers may use the instruments of assessment that are considered by the tutor to be the most appropriate. The student's knowledge of logic symbols can be assessed both explicitly by short answer questions and implicitly as they arise in other performance criteria and outcomes.

REFERENCES

1. Guide to unit writing.
2. For a fuller discussion on assessment issues, please refer to SQA's Guide to Assessment.
3. Information for centres on SQA's operating procedures is contained in SQA's Guide to Procedures.
4. For details of other SQA publications, please consult SQA's publications list.

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