



Unit Assessment Record (UAR)

Sequential Logic and Circuits (D3RC 04)

Credit Value: 1.0

NB: After entering your personal details please pass this document to your tutor for completion and eventual return to COLU. You may wish to retain a copy for your own use.

TITLE:	SURNAME:	UNIT TUTOR:	
FORENAME(s):	CENTRE:		
HOME ADDRESS:	ADDRESS:		
.....		
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POST CODE:	POST CODE:		
HOME TEL:	TEL NO:		
WORK TEL:	FAX NO:		
FAX NO:	E-MAIL:		
E-MAIL:	CENTRE CONTACT:		
SQA REG. NO:		UNIT START DATE:	
<u>AUTHENTICATION OF EVIDENCE – INTERVIEW</u>		DATE:	
PORTFOLIO OF EVIDENCE AVAILABLE	<input type="checkbox"/>		
EVIDENCE AUTHENTICATED	<input type="checkbox"/>		
ALL OUTCOMES SATISFIED	<input type="checkbox"/>		
Please initial as appropriate			
NOTES:			
.....			
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<u>GRADE</u>			
	REFER	PASS	MERIT
FINAL GRADE:	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Please initial as appropriate			
ASSESSOR:		DATE:	

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VERIFIER:..... DATE:

Evidence Log – For each of the performance criteria please clearly identify the evidence within the portfolio that satisfies the criterion fully with respect to range and evidence requirements as stated in the unit specification.

1) Specify the properties of sequential logic circuits

TMA Evidence

Supplementary Evidence & Location

- | |
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| (a) Classification of sequential logic is correct in terms of synchronous and asynchronous working. |
| (b) Interpretation of the current National Standard for graphical symbols of binary logic elements is correct. |
| (c) The behaviour of a bistable element is correctly described using appropriate representation. |
| (d) Integrated circuit packages are used to demonstrate the operation of J-K and type-D bistables. |

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2) Apply formal design techniques to synchronous sequential logic circuits

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| (a) Sequential behaviour of a specification is verified by a state diagram from a given starting state and a sequence of input values. |
| (b) A state-transition table is correctly constructed from a specification's state diagram. |
| (c) The minimum number of binary elements is determined exactly from the number of internal system states. |
| (d) Next-state and output functions are derived and minimized. |
| (e) Logic diagrams are drawn correctly in terms of function and drawing convention. |

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3) Implement sequential logic design projects using integrated circuit devices

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| (a) Manufacturers' data for selected integrated devices are correctly interpreted. |
| (b) Block diagrams drawn for the proposed system accurately represent the required specification. |
| (c) Supporting and driving logic requirements are derived from design equations. |
| (d) The realised design is built, tested and verified as functioning according to specification. |

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Assessment Matrix – The matrix indicates which instruments of assessment, within the primary assessment package, are required to satisfy individual performance criteria.

The column titled **Merit** identifies where particular opportunities exist for candidates to develop their work with a view to satisfying the requirements for the award of merit.

The row titled **Minimum Evidence Requirement** indicates the minimum number of examples required (or times a task must be performed) to satisfy a particular performance criterion.

Sequential Logic and Circuits

OUTCOMES/PERFORMANCE CRITERIA		Qu	1a	1b	1c	1d	2a	2b	2c	2d	2e	3a	3b	3c	3d	Merit	
EVIDENCE	TMA - 1 (v2)	1		X													
		2			X												
		3			X												
		4			X												
		5		X					X	X							
	TMA - 2 (v2)	1							X		X						
		2					X				X						
		3			X												
		4				X											
		5							X	X	X	X					
	TMA - 3 (v2)	1						X	X	X	X	X					
		2					X				X						
		3						X									
		4					X	X	X	X	X						
	PROJECT (v2)						X						X	X	X	X	X
	MINIMUM EVIDENCE REQUIREMENT			1	2	4	1	3	3	5	6	3	1	1	1	1	1

Merit Statement

To gain a pass in this unit, a candidate must meet the standards set out in the outcomes, performance criteria, range statements and evidence requirements.

To achieve a merit in this unit, a candidate must demonstrate a superior or more sophisticated level of performance. In this unit this might be shown in the following ways:

- (a) using the individual performance criteria in a creative way to solve unfamiliar problems by the transfer of a competence gained in one situation to a related but unfamiliar situation
- (b) demonstrating a critical awareness of the relation of theory to the practical development of the subject when, for example, implementing a sequential design
- (c) research outside the normal course content.